PATENT APPLICATION
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chan-Yong LEE, et al.

Serial No. 10/002,542 Examiner: Le, Thong Quoc

Filed: November 13, 2001 Group Art Unit: 2818

For: SENSE AMPLIFIER FOR MEMORY DEVICE

BOX NON FEE AMENDMENT
Assistant Commissioner for Patents
Washington, D.C. 20231

RESPONSE TO OFFICE ACTION

Responsive to the Office Action mailed on July 23, 2002, please amend the application as follows.

IN THE SPECIFICATION

Please replace the paragraph beginning page 4, line 28 to 33 with the following:

FIG. 6 shows an embodiment of data path structure having a new high-speed Bit Line Sensing Amplifier (BLSA) for a semiconductor memory device. The BLSA includes a PSA, NSA, RSA, DIOG4, RCSL, WCSL, DIO/DIOB, etc. that operate in a manner as described above. One difference between FIG. 6 and FIG. 5 is the DIOG4. The DIOG4 only has two transistors, N15, N16. This reduces layout area in the memory core. Core refers to a portion of the memory cell arrays, Bit Lines (BLs), BLSA, and Word Line related circuits, etc.

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Please replace the paragraph beginning page 6, line 14 to line 23 with the following:

FIG. 12 shows another embodiment where a Mode Register Set (MRS) command or signal is generated in the DRAM right after power-up. The MRS may be programmed after power-up and before normal operation. In addition, the MRS may also be changed during normal operation. The MRS command or signal is applied for initially determining how the DRAM operates. The MRS signal sets CL (CAS Latency), BL (Burst Length), etc., and is a combination of external command signals (CLOCK, CSB, RASB, CASB, WEB) and a plurality of addresses. The CSB signal refers to a chip select signal and the RASB signals refers to a row address strobe signal. The CASB signals refers to a column address strobe

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